PNSQC

OCTOBER 10-12 2022

Mohamed A. Bahnasawi

Risk-based testing for EDA tools

Agenda

- Biography
- Integrated-Circuit (IC) Industry
- EDA innovation in IC industry
- Quality in EDA is a MUST
- Risk-based testing (RBT) Approach
- Brief to the tested tools
- RBT Results
- Conclusion

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Biography

- Mohamed Bahnasawi was graduated from Cairo University, Egypt in 2016 and his graduation project was implementation of Embedded Systems GPU.
- He is a Senior Software QA Engineer at Siemens EDA with 5 years of experience in automation and testing.
- He has 5 published research paper in Electronics and EDA testing fields

Biography

- Ahmed Khater was graduated from Ain Shams University, Egypt in 2007
- He is a QA Team Lead at Siemens EDA with 14 years of experience in Software Developments and Testing Process

Biography

- Reem ElAdawi holds a BSc., Msc. And Phd from Ain Shams University, Egypt.
- She is a Test Engineer Director at Siemens EDA with 25+ years of experience in Software Development and Testing Process.
- She has multiple publications related to machine learning applications.

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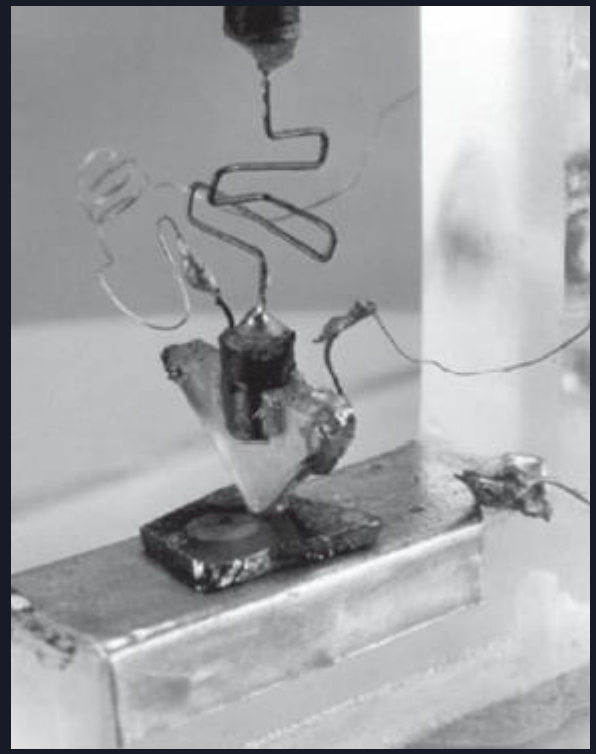
Integrated-Circuit (IC) Industry

- First Transistor was built in 1947 John Bardeen and Walter Brattain built at Bell Labs.



First transistor in 1947

Integrated-Circuit (IC) Industry

- First Transistor was built in 1947 John Bardeen and Walter Brattain built at Bell Labs*
- In 1959, Bell labs invented the (MOSFET)** transistor by Mohamed M. Atalla and Dawon Kahng and it was the dominant transistor type in use until 2020

MOSFET Transistor

* Bell Labs is the research arm of AT&T and now is a part of Nokia

** MOSFET tends to Metal-Oxide Semiconductor Field Effect Transistor

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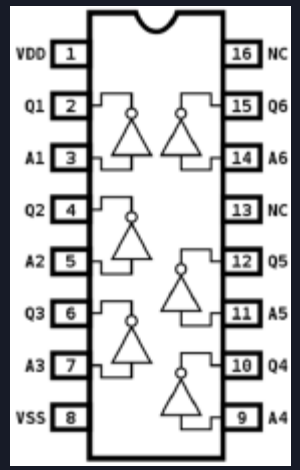
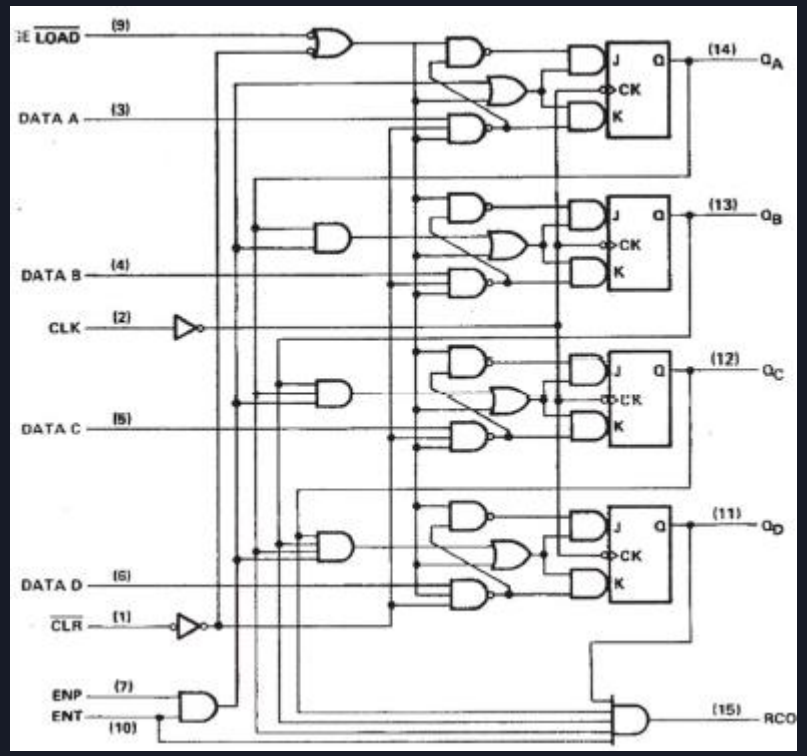
Integrated-Circuit (IC) Industry

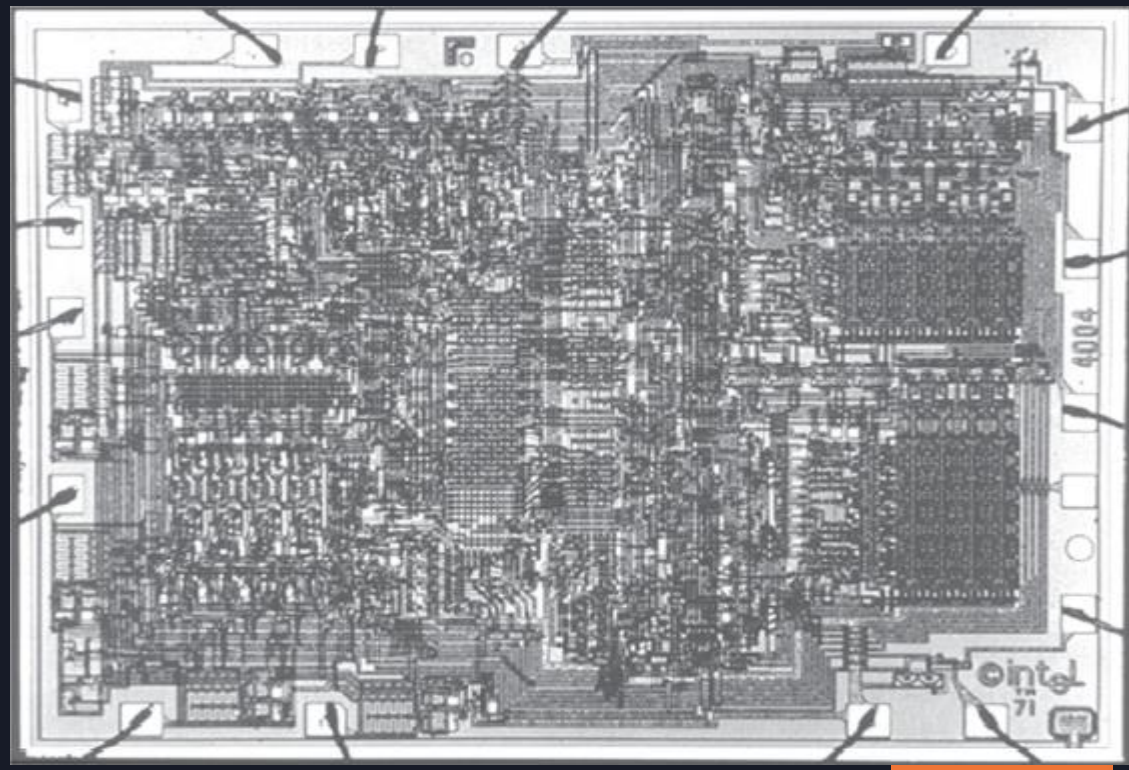
Small Scale Integration (SSI) ~10 gates



Medium Scale Integration (MSI) ~1000 gates



Large Scale Integration (LSI) ~10,000 gates



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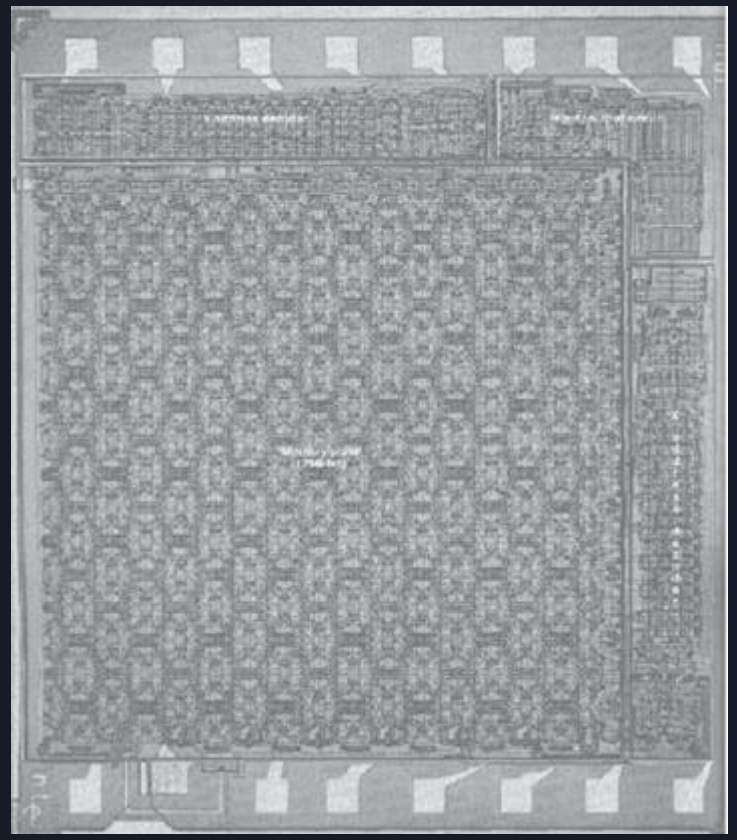
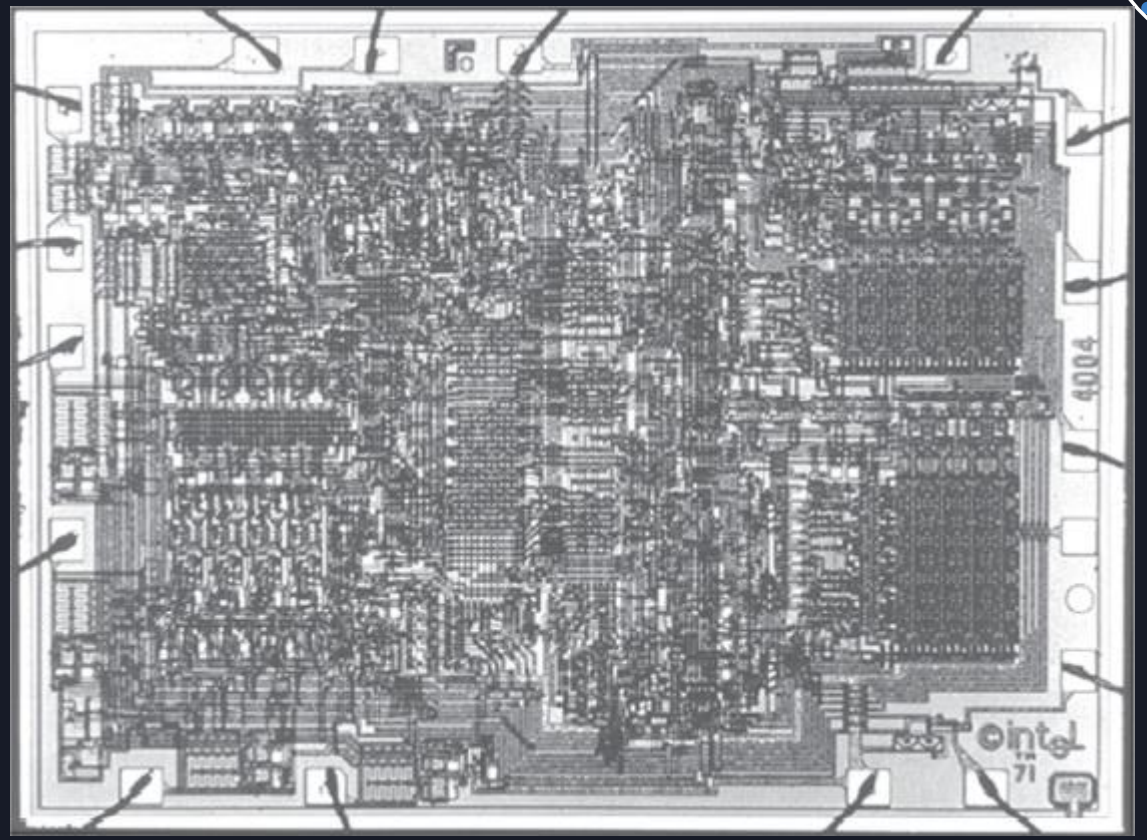
Integrated-Circuit (IC) Industry

- In 1970s



Intel 1101 SRAM – 256-bit memory



4004 4-bit microprocessor

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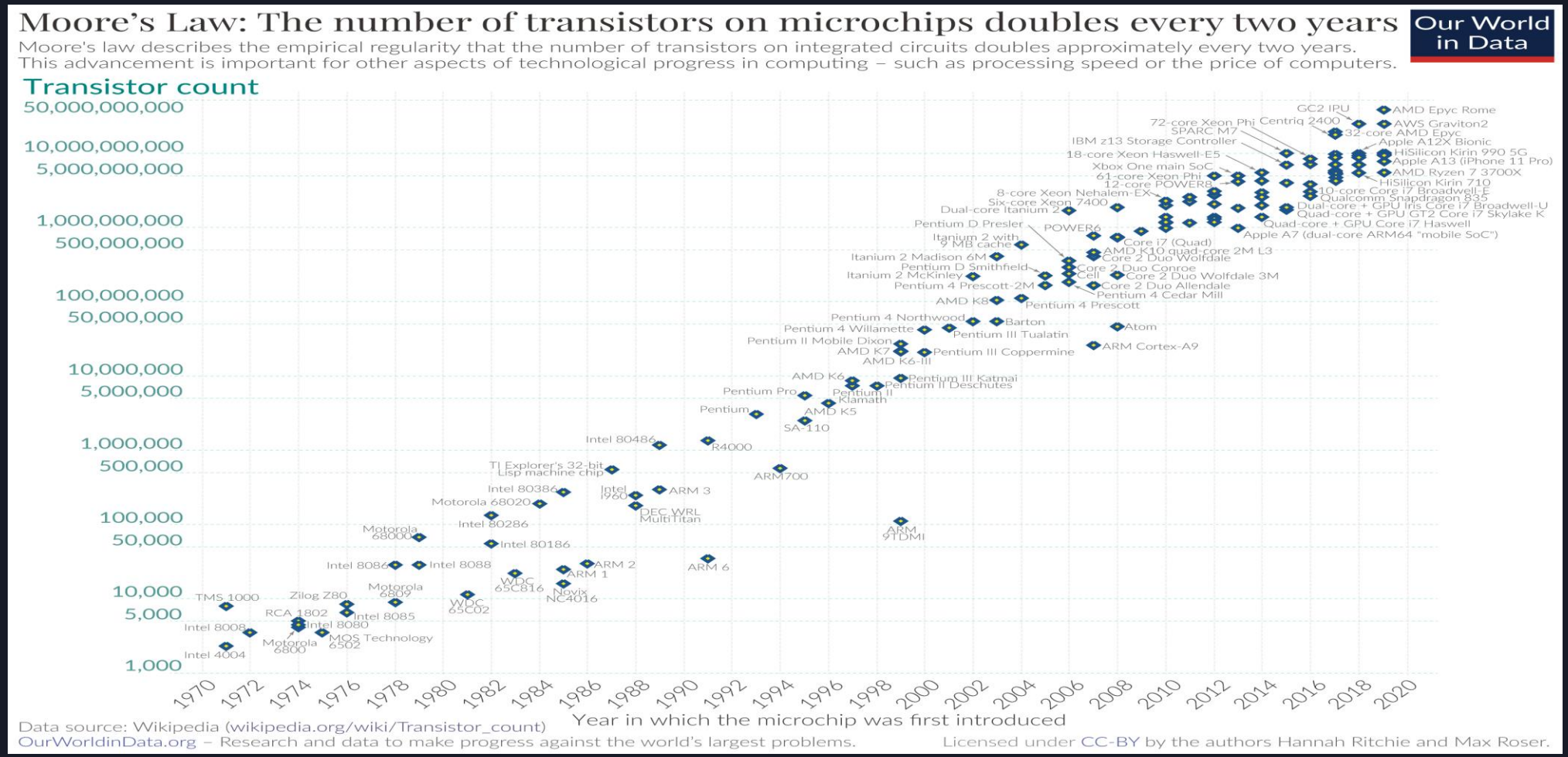

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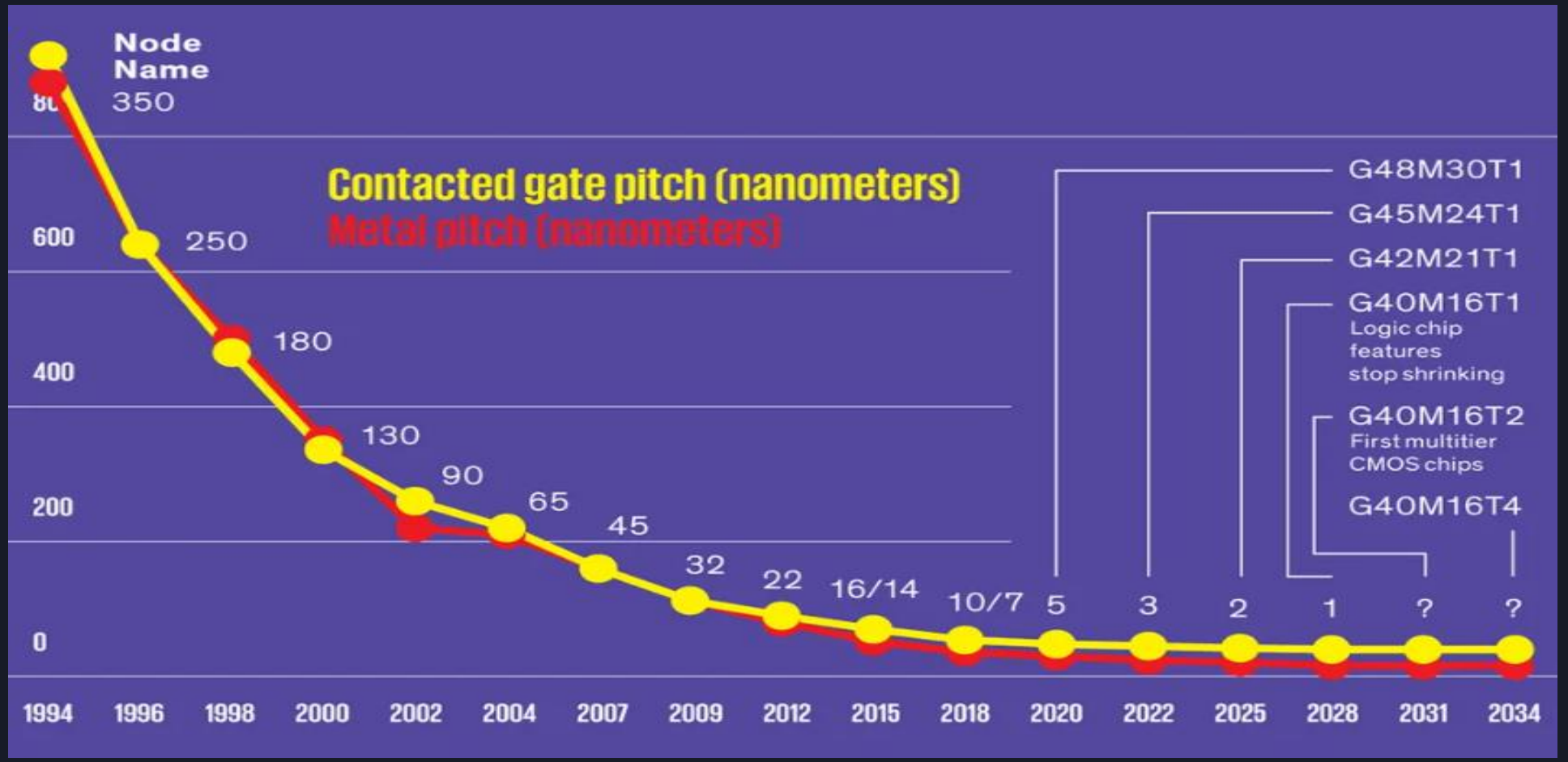

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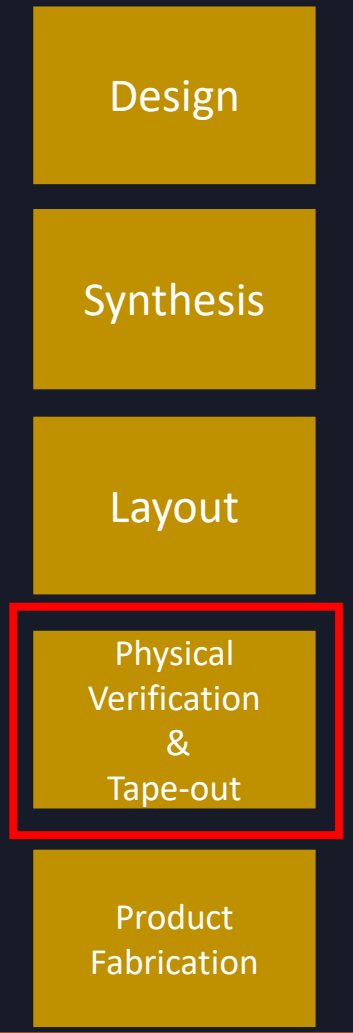
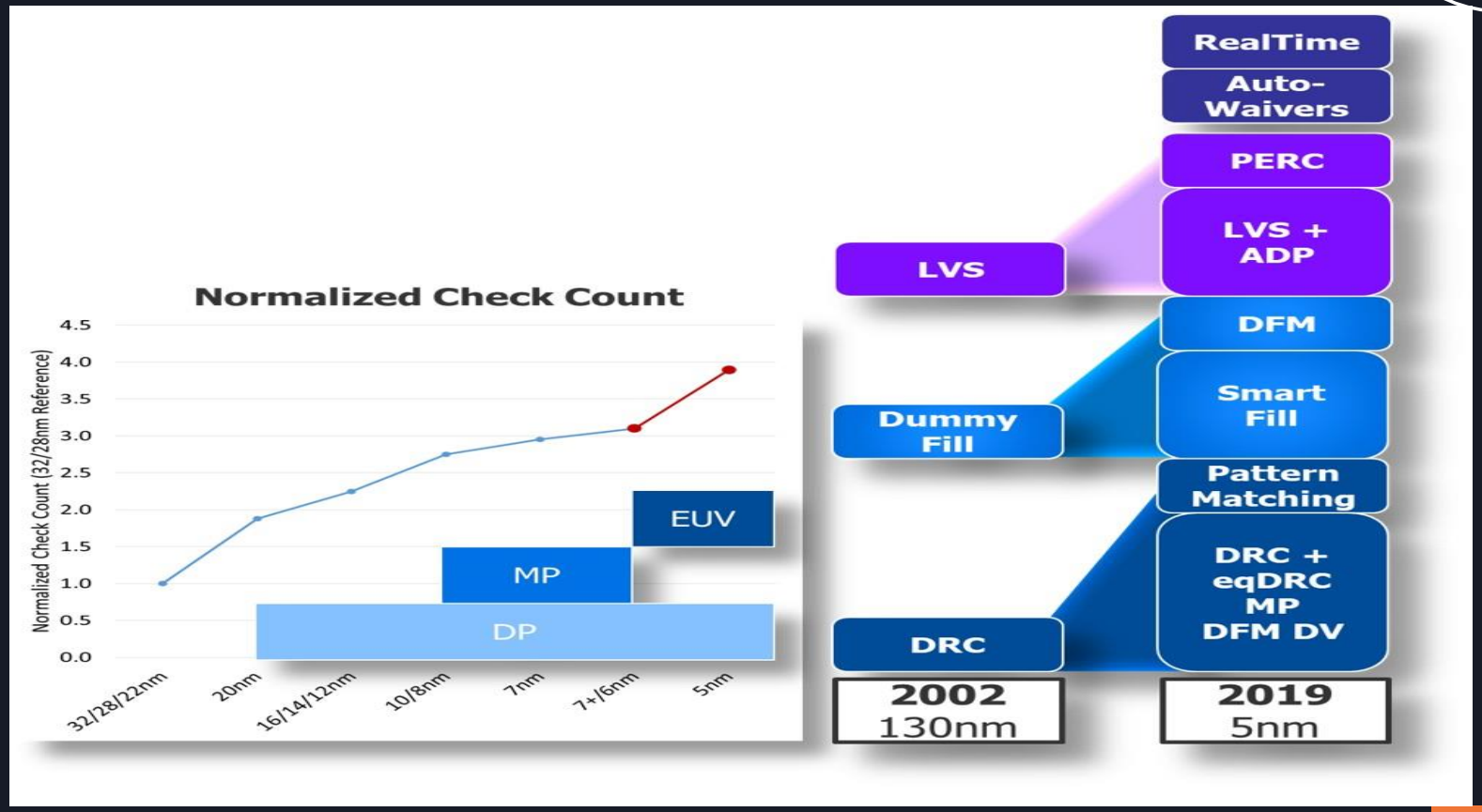
EDA innovation in IC industry

Before EDA (Electronic Design Automation) industry ?

- Layers were hand drawn, checked with magnifying glasses, manually checked for design rules and layout vs. schematic checks
- The first Intel product, the 3101 64-bit RAM was actually a 63-bit RAM due to a cutting error

EDA innovation in IC industry





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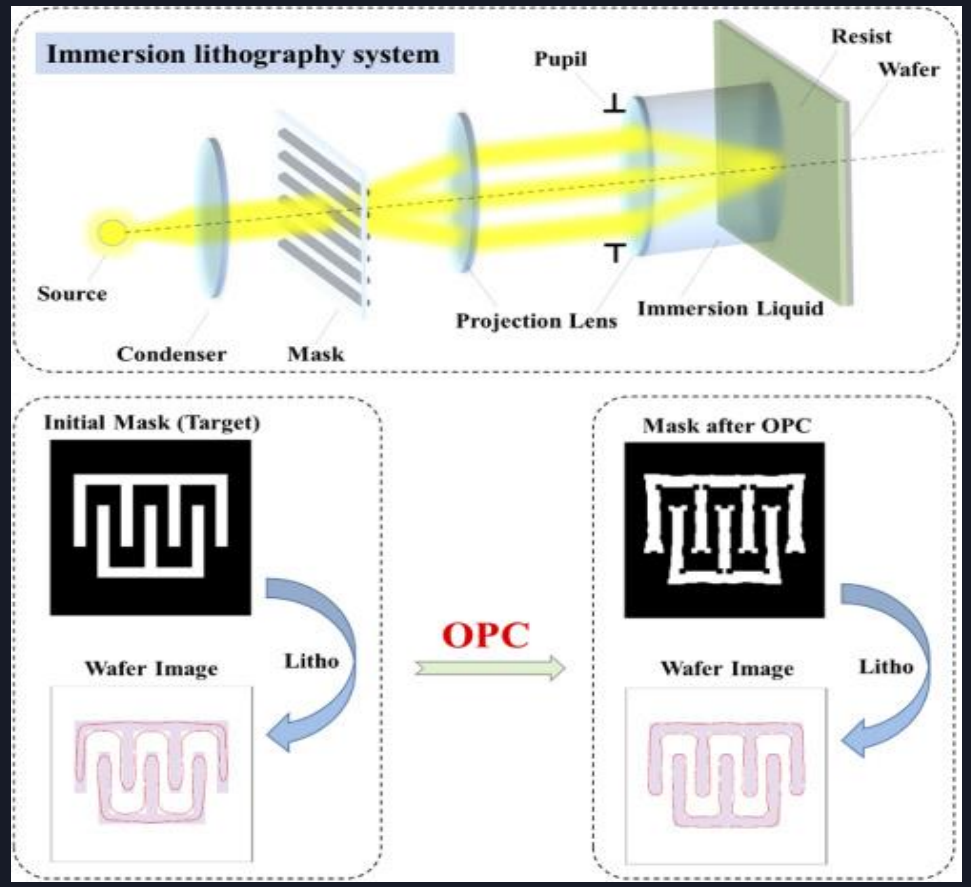
EDA innovation in IC industry

For Fab side:

- IC fabrication depends mainly on crossing light through masks then projection lens to draw layers in range of nm.
- Light diffraction wave length is 130 um .
- Using EDA to enhance resolution



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Quality in EDA is a MUST

- Some hardware defects cost hundred of millions dollars

20 December	In response to a firestorm of public opinion, Intel announces plans for a total recall, replacement, and destruction of the flawed Pentium processors.
17 Jan 1995	Intel announces a pre-tax charge of 475 million dollars against earnings, ostensibly the total cost associated with replacement of the flawed processors.

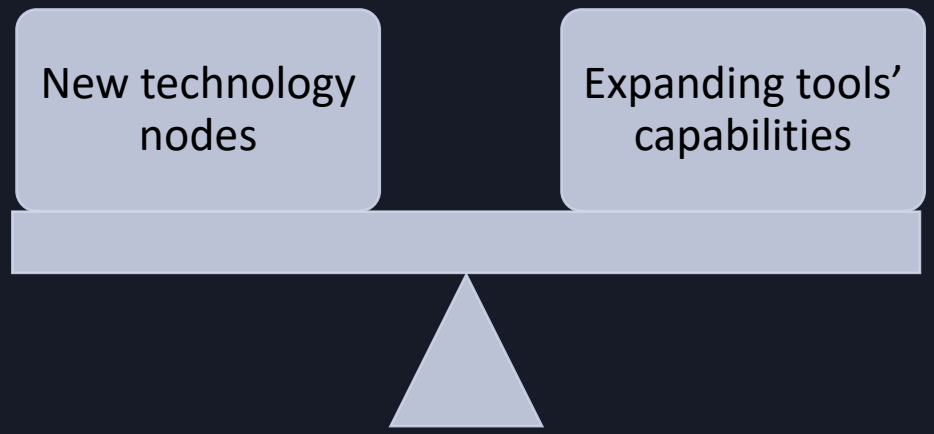
The growing dissatisfaction with Intel's response led to the company offering to replace all flawed Pentium processors on request on December 20.[14] On January 17, 1995, Intel announced "a pre-tax charge of $475 million against earnings, ostensibly the total cost associated with replacement of the flawed processors."[9] This is equivalent to $752 million in 2020.[15] Intel was criticised for barring resellers and OEMs from participating in the recall program, requiring end-users to replace chips themselves. Intel's justification for this, posted on its support web page, was that "it is the individual decision of the end user to determine if the flaw is affecting their application accuracy".[13]

- As IC industry is mainly depending on EDA tools, so quality in EDA is not a choice. It is a MUST !!

Quality in EDA is a MUST

EDA Dilemma:

- Balancing between new technology nodes and introducing new capabilities to the tool.
- This is to meet the fast growth in IC industry
- All of that with respect to the **QUALITY**



Quality in EDA is a MUST

- To meet the tough deadlines with high quality, it is necessary to develop a strategy for prioritizing efforts and allocating resources.
- Risk-based testing (RBT) is used to drive all phases of testing process while reducing testing costs.
- This is without affecting the quality of the tested tools.

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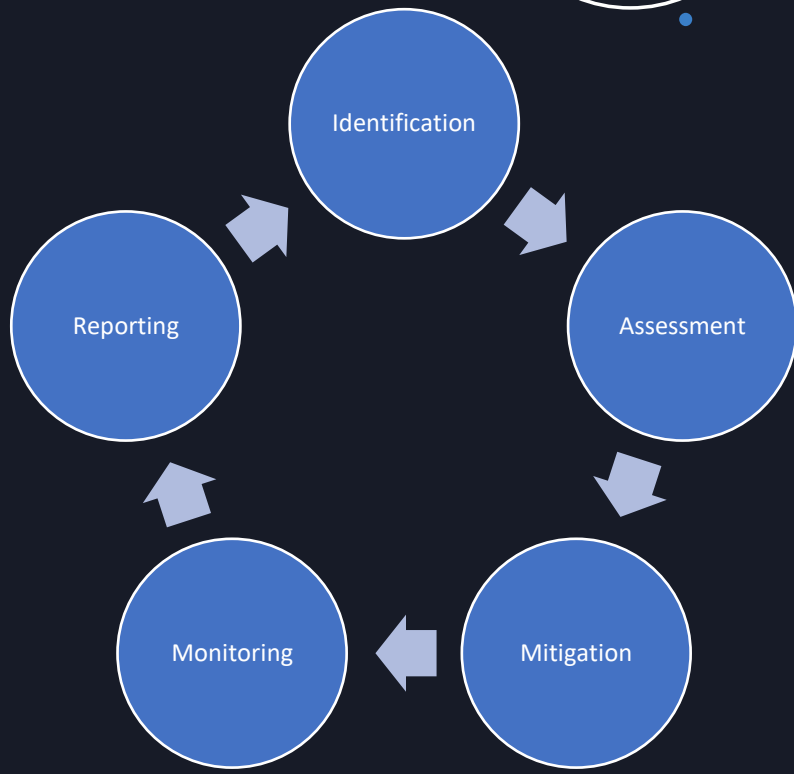
Risk-based testing (RBT) Approach

- Risk Identification
- Risk Assessment
- Risk Mitigation
- Risk Monitoring
- Risk Reporting



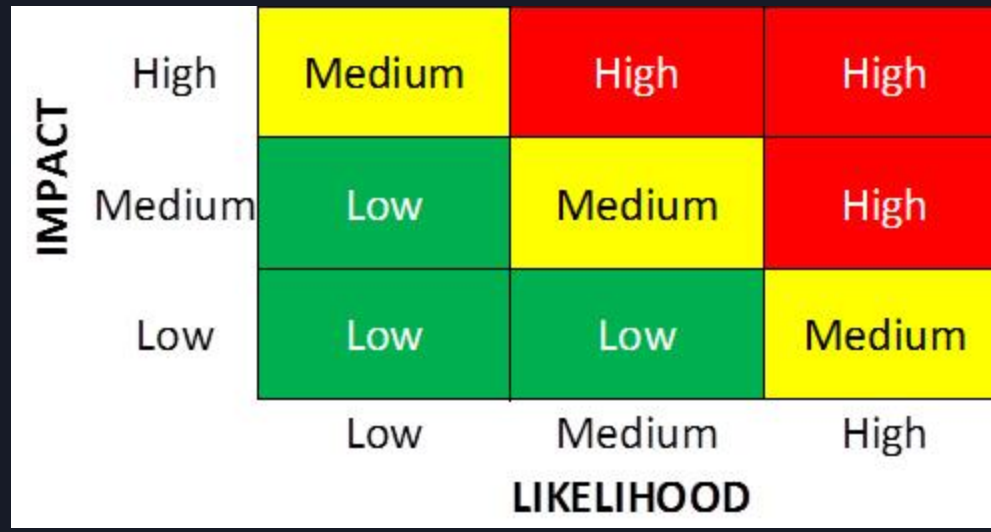
Risk-based testing (RBT) Approach

- Risk Assessment
  QA team to identify risks

Category	Scenario
Functional	Test both sides forbidden cells on cell 1x height (On borders and in the middle of the array)
Functional	Test both sides forbidden cells on multi height cell (On borders and in the middle of the array)
Functional	All filler cells are forbidden from right
Functional	Test forbidden cells with wide cells
Functional	Test the usage of forbidden row number on cell 1x height (make sure that it has no effect)
Functional	Test forbidden cells on arrays with width 1x (rules will not be applied)
Integration	Test with/out includeEveryInputCell
Integration	Generate GDS and OASIS
Integration	Test with includeEveryInputCell and make some cells not appear
Negative	Using wrong file path
Negative	Assign text, negative and floating numbers to forbidden row numbers
Negative	Test forbidden cells in coloring mode
Negative	Test using combination of forbidden row numbers (in range & out of range)
Performance	Repeat test cases of 5x, 6x and 7x with forbidden cells and check runtime and memory differences
Performance	Repeat previous test with more forbidden cells rules

Risk-based testing (RBT) Approach

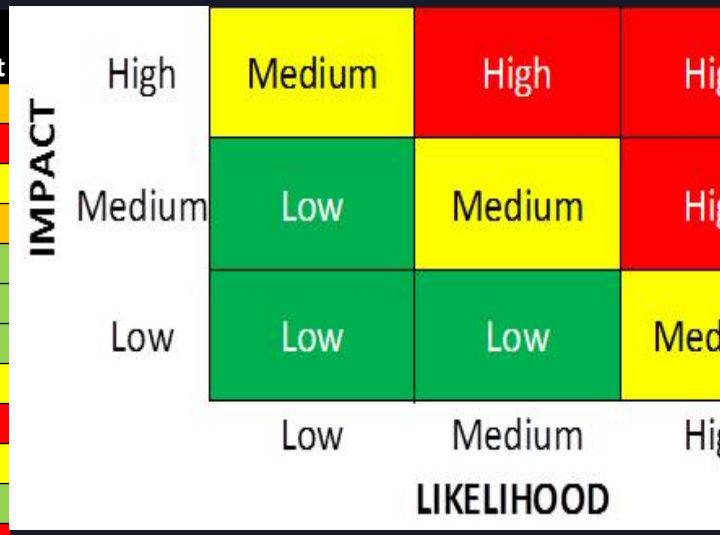
- Risk Assessment
  - Likelihood Factors: It comprises assessing the risk based on
    - software complexity
    - frequency of usage
    - potential defect locations
    - integration between legacy and new features
  - The impact factor is determined based on
    - the criticality of the risk to the customer
    - the absence of solutions
    - the customer's reliance on such a flow



Risk-based testing (RBT) Approach

- Risk Assessment

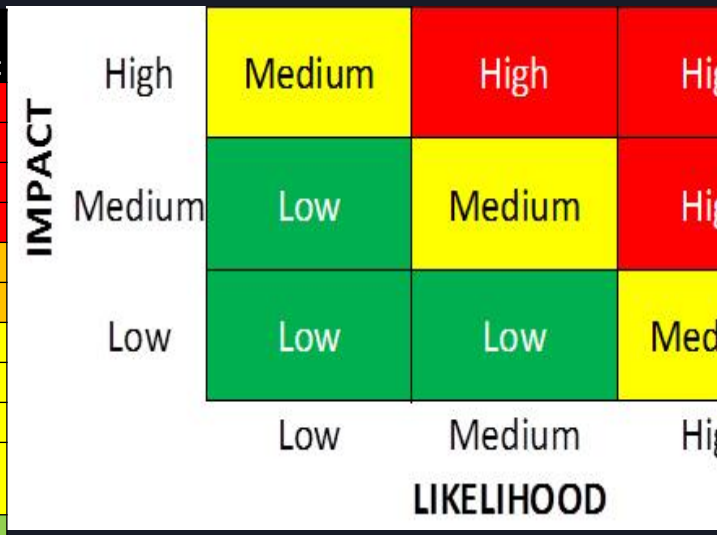
Category	Scenario	Impact	Likelihood	Priority	Risk Assesment
Functional	Test both sides forbidden cells on cell 1x height (On borders and in the middle of the array)	2	3	6	High
Functional	Test both sides forbidden cells on multi height cell (On borders and in the middle of the array)	3	3	9	Critical
Functional	All filler cells are forbidden from right	2	2	4	Med
Functional	Test forbidden cells with wide cells	3	2	6	High
Functional	Test the usage of forbidden row number on cell 1x height (make sure that it has no effect)	1	2	2	Low
Functional	Test forbidden cells on arrays with width 1x (rules will not be applied)	1	1	1	Low
Integration	Test with/out includeEveryInputCell	2	1	2	Low
Integration	Generate GDS and OASIS	2	2	4	Med
Integration	Test with includeEveryInputCell and make some cells not appear	3	3	9	Critical
Negative	Using wrong file path	2	2	4	Med
Negative	Assign text, negative and floating numbers to forbidden row numbers	1	2	2	Low
Negative	Test forbidden cells in coloring mode	3	3	9	Critical
Negative	Test using combination of forbidden row numbers (in range & out of range)	1	1	1	Low
Performance	Repeat test cases of 5x, 6x and 7x with forbidden cells and check runtime and memory differences			0	Low
Performance	Repeat previous test with more forbidden cells rules			0	Low



Risk-based testing (RBT) Approach

- Risk Assessment

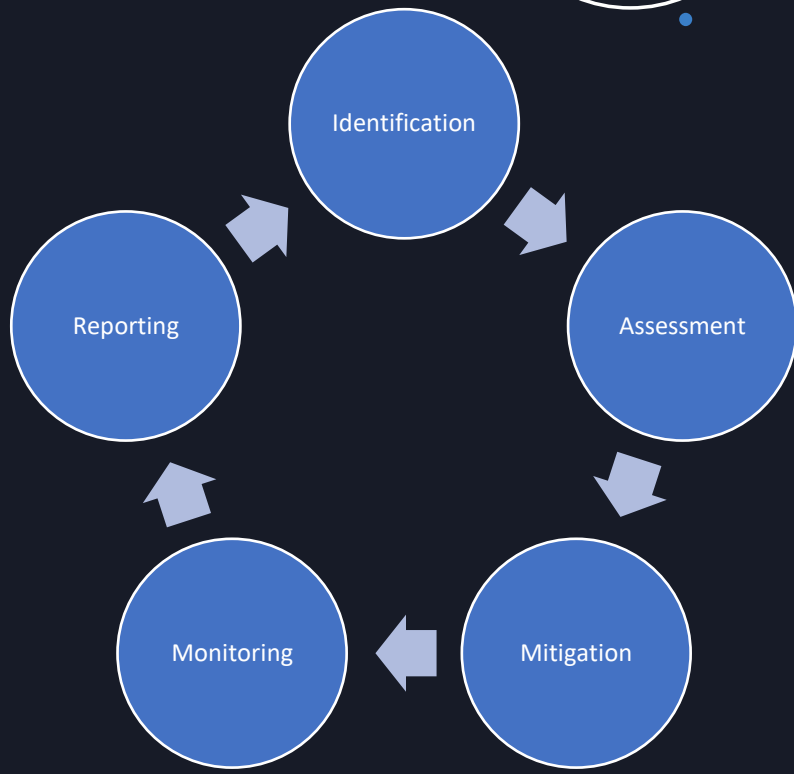
Category	Scenario	Impact	Likelihood	Priority	Risk Assesment
Functional	Test both sides forbidden cells on multi height cell (On borders and in the middle of the array)	3	3	9	Critical
Integration	Test with includeEveryInputCell and make some cells not appear	3	3	9	Critical
Negative	Test forbidden cells in coloring mode	3	3	9	Critical
Performance	Repeat previous test with more forbidden cells rules	3	3	9	Critical
Functional	Test both sides forbidden cells on cell 1x height (On borders and in the middle of the array)	2	3	6	High
Functional	Test forbidden cells with wide cells	3	2	6	High
Functional	All filler cells are forbidden from right	2	2	4	Med
Integration	Generate GDS and OASIS	2	2	4	Med
Negative	Using wrong file path	2	2	4	Med
Performance	Repeat test cases of 5x, 6x and 7x with forbidden cells and check runtime and memory differences	2	2	4	Med
Functional	Test the usage of forbidden row number on cell 1x height (make sure that it has no effect)	1	2	2	Low
Integration	Test with/out includeEveryInputCell	2	1	2	Low
Negative	Assign text, negative and floating numbers to forbidden row numbers	1	2	2	Low
Functional	Test forbidden cells on arrays with width 1x (rules will not be applied)	1	1	1	Low
Negative	Test using combination of forbidden row numbers (in range & out of range)	1	1	1	Low



Risk-based testing (RBT) Approach

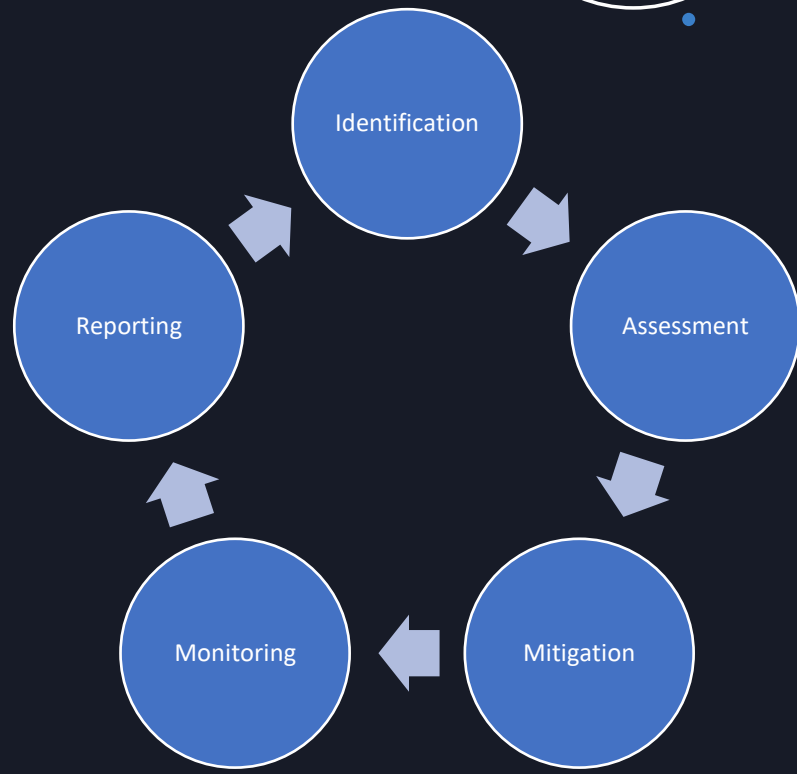
- Risk Mitigation:

Test are designed, implemented, executed to cover the Risk



Risk-based testing (RBT) Approach

- Risk Monitoring and reporting
  - Review the progress of the plan
  - Communicate the effectiveness of test plan to stakeholders
  - Is there a need to change the testing strategy to meet the deadlines ?
    - Risk Reduction: to continue the testing activities for covering more scenarios
    - Risk Avoidance: to avoid engaging in a feature or product
    - Risk Transfer, which is accomplished by outsourcing testing to a third party.
    - Risk Acceptance entails deciding not to deal with the risk or taking no action in response to it.



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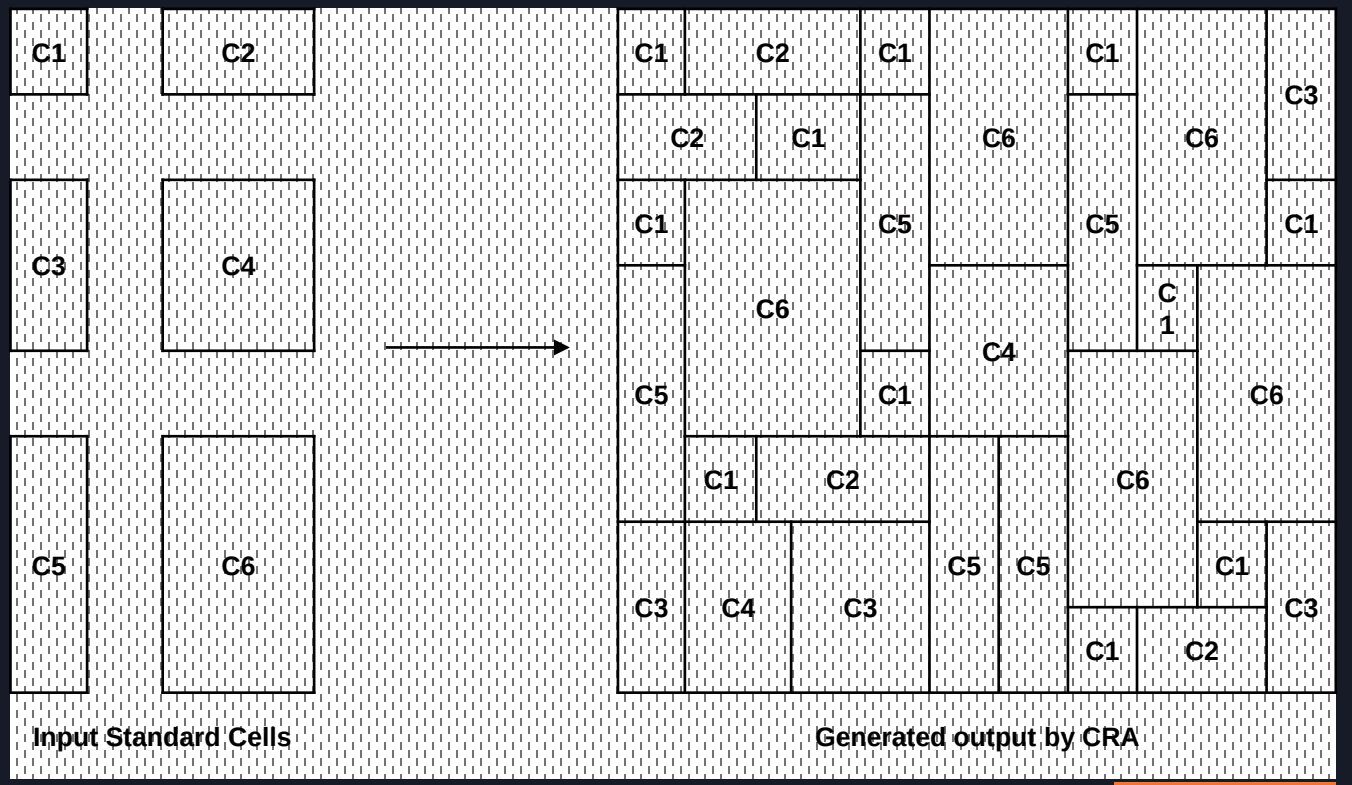
Brief to the tested tools

- For developing new technology nodes, it is necessary to have several layouts for process calibration.
- This is to test the fabrication rules like DRC “Design Rule check” before using these rules on realistic layouts.
- Check the ability of fabrication machines to fabricate specific shapes.

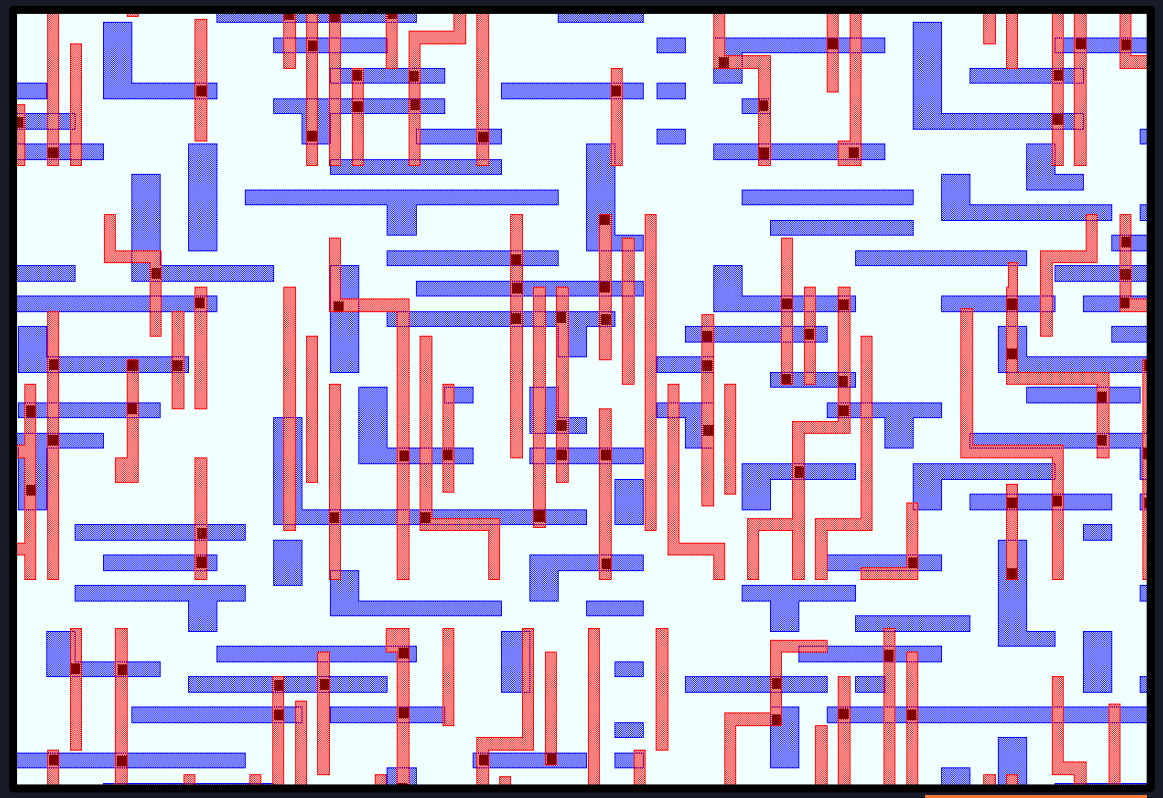
Brief to the tested tools

- CRA “Create Random-Cell Array”
  - CRA is a utility that creates random placements of standard cells.
  - CRA aids quality assurance of standard cell libraries including hundreds or thousands of cells



Brief to the tested tools

- VRP “VIA Random Placement”
  - The VRP flow generates and places vias in the design layout at random using a set of input criteria
  - Using the VRP flow allows designers to do early pattern analysis



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RBT Results (CRA)

Risk Assessment	Testing Categories				Total
	Functional	Integration	Performance	Negative	
Critical	4	5	3	3	15
High	5	0	1	0	6
Med	7	1	0	3	11
Low	3	0	0	1	4
Total	19	6	4	7	36

Risk Assessment for CRA

Testing Activity	Time in mins
Risk Identification	~60
Risk Assessment	~30
Prepare the testing environment & input data	~480 (1 working day)
Testing scenarios for each risk including automation	~53-70 (Depending on scenario's complexity)
Total	~2370 (5 working days)

Time planning for CRA

RBT Results (CRA)

- The overhead time is less than 4% of total time.
- During the Critical Risks testing, 5 bugs were discovered
- As a result of the early detection of these bugs, the development team had more time to fix them to meet the release cycle
- some lower priority features received only partial testing so stakeholders preferred protecting them with beta variable
- Performance testing started in very early stage as it was a need to the customer

RBT Results (VRD)

Risk Assessment	Testing Categories				Total
	Functional	Integration	Performance	Negative	
Critical	6	5	0	2	13
High	3	0	0	6	9
Med	0	1	0	0	1
Low	1	0	2	2	5
Total	10	6	2	10	28

Risk Assessment for VRD

Testing Activity	Time in mins
Risk Identification	~60
Risk Assessment	~20
Prepare the testing environment & input data	~240 (0.5 working day)
Testing scenarios for each risk including automation	~20-60 (Depending on scenario's complexity)
Total	~1440 (3 working days)

Time planning for VRD

RBT Results (VRD)

- The overhead time is less than 6% of total time.
- During the Risk Identification process, there is a scenario that is not well stated in the requirements documents and functional specifications
- The bug identified in very early stage
- RBT was reporting at an early stage the satisfaction of the testing team with the tool quality, and it can be used in reallocating resources for testing other low-quality tools.

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Conclusion

- RBT focuses on flows that are more likely to fail or are more vital to the customers.
- RBT allows stakeholders to make early decisions to lower the risk of the delivered feature, hence shortening their time to market.
- The overhead in adding RBT to the testing process is around 4-6% of the total time planned for the full testing process.
- Instead of blindly following traditional testing process, such as applying performance testing at the end, RBT raised awareness of the critical need for high performance
- The order of testing became dependent on the customer's needs and the risky flows.

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THANK YOU